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CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German application DE 101 11 462.1, filed with the German Patent Office on March 9, 2001.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Thyristor structure and overvoltage protection arrangement having such a thyristor structure

The invention relates to a thyristor structure and an overvoltage protection arrangement in accordance with Patent Claims 1 and 4.

Nowadays, thyristor structures having a planar structure are customary when using CMOS technologies. A thyristor structure of this type is shown, in principle in Fig. 3. At the surface of such a component, an n^--type region 2 and a p^--type region 3 are arranged such that they lie next to one another, which regions also form the so-called base regions of the thyristor structure. A p^+-type region 1, which represents the anode terminal, is formed in the n^--type region 2. An n^+-type region 4 formed in the p^+-type region 3 represents the cathode terminal. A p^+-type region 5 formed in the p^--type region 3 in turn forms the control terminal.

In the production of the structure described above, a nitride layer is applied to the surface 8. Charges in said nitride layer lead to a parasitic field effect. The same parasitic effect occurs if, at the surface 8, contaminants are incorporated in the regions 2 and 3 during production.

The thyristor structure described above is employed particularly frequently in overvoltage protection arrangements for a so-called ESD protection. The latter is frequently employed in MOS input stages of integrated circuits. An overvoltage detector is arranged at that part of the integrated circuit which is to be protected, said overvoltage

detector being connected to the control terminal of the thyristor. An arrangement of this type is described in US 4,896,243.

The anode and cathode of the thyristor are in turn connected to the supply voltage of the component to be protected, if the supply voltage is to be monitored.

If an overvoltage then occurs, switched on via the control overvoltage is conducted away.

If the parasitic field-effect transistor, as described above, is then formed, the monitored voltage *is* short-circuited, which leads to the total failure of the component to be protected.

The invention is based on the object of developing a thyristor structure and an overvoltage protection arrangement having such a thyristor structure in such a way that the influence of parasitic effects is avoided.

This object is achieved according to the invention by means of the measures specified in the coordinate patent claims.

By forming at least one auxiliary electrode at the surface of one of the two regions of the second and third regions, it is possible to put the surface in the region of the auxiliary electrode into a predetermined charge state.

An overvoltage protection arrangement having such a thyristor structure does not lead to the failure of the components to be protected as a result of parasitic effects.

Further advantageous refinements of the invention are specified in the subordinate claims.

By providing an auxiliary electrode in each case on the second and third regions and connecting the auxiliary electrodes on the second region to the first terminal and the auxiliary electrode at the third region to the second terminal. the predetermined charge states can be produced at the surface in a simple manner.

By forming the auxiliary electrode with polysilicon and a gate oxide which isolates the latter from the second and third regions, the auxiliary electrode can be produced in a simple manner using a customary technology.

By integrating the overvoltage protection arrangement on a semiconductor chip. the overvoltage protection can be produced simply and effectively.

The invention is explained below using embodiments with reference to the drawings.

In the figures:

Fig. 1 shows a thyristor structure according to the invention,

Fig. 2 shows an overvoltage protection arrangement according to the invention in a basic illustration, and

Fig. 3 shows a customary thyristor structure.

Fig. 1 shows an exemplary embodiment according to the invention of a thyristor structure which, in principle,

corresponds to that which has already been explained in the introduction to the description with reference to Fig. 3. In this case, identical parts are provided with identical reference symbols.

In the exemplary embodiment illustrated, mutually isolated auxiliary electrodes are additionally formed at the common surface of the second region 2 and third region 3, which are often also referred to as base regions of the thyristor. These auxiliary electrodes are composed of a gate oxide 6, customary for the production of field-effect transistors, and an electrode contact 7 made of polysilicon. The electrode contact 7 of the auxiliary electrode which is formed at the surface of the surface region 2 is electrically conductively connected to the first terminal 1, the anode contact. The auxiliary electrode which is formed at the third region 3 is electrically conductively connected to the second terminal, the cathode contact. This ensures that a conductive channel which would bring about a short circuit between first terminal 1 and second terminal 3 cannot form at the surface in the base regions as a result of parasitic effects. The thyristor structure is turned on only by a current being impressed at the control terminal 5.

Fig. 3 shows a basic illustration of the thyristor structure in an overvoltage arrangement. The thyristor structure described above is connected by its anode and cathode terminals. i.e. by the first terminal 1 and the second terminal 3, to the supply voltage VDD and VSS of the component 11 to be protected. An overvoltage detector device 13 monitors the supply voltage of the component 11 to be protected. When an overvoltage occurs, the overvoltage detector device 13 impresses a current via the control terminalS into a base

region, namely the third region 3, of the thyristor structure. The latter triggers and short-circuits the supply voltage.

The arrangement is particularly suitable for integration. This means that the thyristor structure is integrated. together with the overvoltage detector at the surface of the component to be detected, the two auxiliary electrodes avoiding the situation where the thyristor structure is arranged below a thick oxide in order to avoid parasitic effects. Consequently, the action of the thyristor structure is completely maintained.

Furthermore, such an arrangement can be applied to other instances of voltage monitoring, such as the voltage of signal inputs.

Patent Claims

1. Thyristor structure having
- a first terminal (1) formed as a first region with a first conductivity type,
- a second region (2) of a second conductivity type, which adjoins the first region (1),
- a third region (3) of the first conductivity type, which adjoins the second region (2) and has a common surface (7) with the latter, and
- a second terminal (4), which, as fourth region of the second conductivity type, adjoins the third region,

characterized in that,
- at the common surface of the second region (2) and the third region (3), an auxiliary electrode (6,7) is arranged in a manner adjoining at least one of the two regions.

2. Thyristor structure according to claim 1, characterized in that, an auxiliary electrode (6,7) is in each case arranged in a manner adjoining the second region (2) and the third region (3) on the common surface (8) of second region (2) and third region (3).

3. Thyristor structure according to claim 1 or 2, characterized in that the auxiliary electrode (6,7) is formed from a conductive region (7) made of polysilicon and an auxiliary oxide which isolates the conductive region (7) from the common surface (8).

4. An overvoltage protection arrangement having a thyristor structure according to one of claims 1 to 3, in which a component (5) to be protected is arranged in an electrically conductive manner between the first terminal (1) and the second terminal (4) and the second or third region (3) has a

control terminal (5), to which is connected an overvoltage detector which detects an overvoltage across the component to be protected.

5. Overvoltage protection arrangement according to claim 4, characterized in that the control terminal (5) is a region of the same conductivity type as the region at which it is arranged, and has a higher conductivity than the latter.

6. Overvoltage protection arrangement according to claim 4 or 5, characterized in that the supply voltage (VDD, VSS) of the component to be protected is connected to the first terminal (1) and the second terminal (4).

7. Overvoltage protection arrangement according to claim 4, 5 or 6, characterized in that the overvoltage protection arrangement is arranged in an integrated manner on a single semiconductor chip.

Abstract

Thyristor structure and overvoltage protection arrangement having such a thyristor structure

A thyristor structure having a first terminal (1), formed as a first region with a first conductivity type, is provided. A second region (2) of a second conductivity type adjoins the first region (1). A third region (3) of the first conductivity type, which adjoins the second region (2), has a common surface (8) with the latter. A second terminal (4), as fourth region of the second conductivity type, adjoins the third region. At the common surface of the second region (2) and the third region (3), an auxiliary electrode (6, 7) is arranged in a manner adjoining at least one of the two regions.

Fig. 1

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